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(University of Choice)

MASINDE MULIRO UNIVERSITY OF SCIENCE AND TECHNOLOGY (MMUST)

UNIVERSITY EXAMINATIONS 2021/2022 ACADEMIC YEAR

FOURTH YEAR SECOND SEMESTER MAIN EXAMINATIONS

FOR THE DEGREE OF BACHELOR OF ENGINEERING ELECTRICAL ENGINEERING

COURSE CODE: SPH 441

COURSE TITLE: DIGITAL SYSTEMS DESIGN

DATE: MONDAY 25TH APRIL, 2022 **TIME:** 12:00 PM - 2:00 PM

INSTRUCTIONS TO CANDIDATES

TIME: 2 Hours

Answer question ONE and any TWO of the remaining.

Symbols used bear the usual meaning.

MMUST observes ZERO tolerance to examination cheating

This Paper Consists of 4 Printed Pages. Please Turn Over.

QUESTION ONE (30 MARKS)

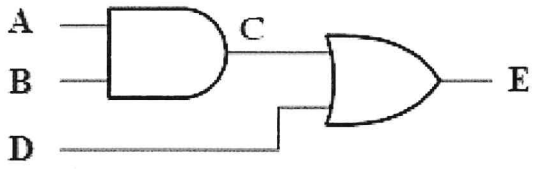
(a). Distinguish between:

(i) Combinational logic circuits and Sequential circuits. **(2marks)**

(ii). Synchronous and asynchronous circuits **(2marks)**

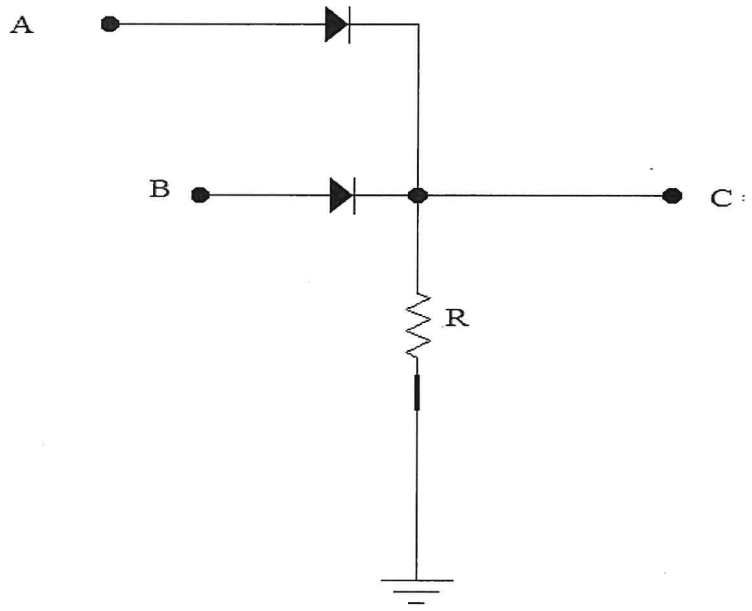
(b) Convert $9AF_{16}$ to its binary equivalence. **(3marks)**

(c). The Figure below shows two logic gates connected together. Write a complete VHDL module for the setup. **(4marks)**



(d). List the three levels essential in VHDL description of digital systems **(3marks)**

(e). The figure below shows a two input logic gate circuit.



(I). Identify the gate and provide its corresponding logic symbol. **(2marks)**

(II). Complete the truth table below under the given conditions for the gate in (e) above:

A	B	C (output)
0	0	
1	0	
0	1	
1	1	

(2marks)

(f). Describe the meaning and development of VHDL as a hardware description language

(4marks)

(g). Demorganize the function $\overline{A.B}$ **(3marks)**

(h). The XOR gate can be used as a binary to Gray-code converter. Using a clear diagram, illustrate the conversion of 1010_2 to its Gray-code equivalent. **(3marks)**

(*i*). Define the following terms:

(I). Real **(1mark)**

(II). Time **(1mark)**

QUESTION TWO (20 MARKS)

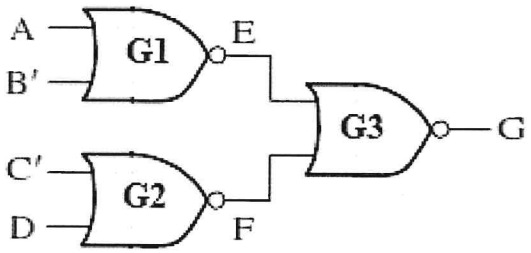
(a).List the two factors that need to be declared when using an array in VHDL **(2marks)**

(b). Give the VHDL Description of a ROM **(18marks)**

QUESTION THREE (20 MARKS)

(a). Using IEEE std_logic, illustrate the VHDL Code for Bi-Directional I/O Pin. **(6marks)**

(b). The Figure below shows a NOR-NOR gate circuit.



Give the corresponding structural VHDL code **(10marks)**

(c). Below is a two dimensional array signal, Y:

$$\begin{bmatrix} 5 & 8 \\ 0 & 4 \end{bmatrix}$$

Describe the array in VHDL. **(4marks)**

QUESTION FOUR (20 MARKS)

(i).

(a). Highlight the concept of Racing in flip-flops. **(5marks)**

(b).

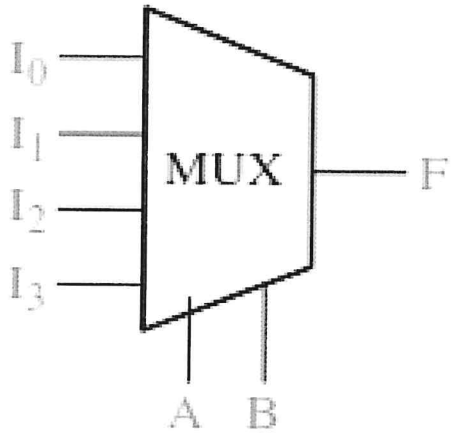
(i). How is Racing alleviated. **(2marks)**

(ii). Discuss the design a multiplier for two 4-bit positive binary numbers. **(13marks)**

QUESTION FIVE (20 MARKS)

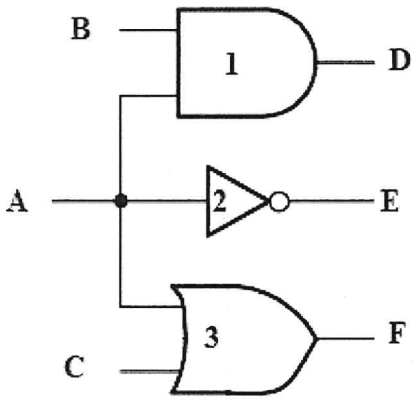
(a). Describe the construction of an SM chart. **(9marks)**

(b). A 4-to-1 MUX has got four data inputs and two control inputs, A and B as shown below.



The control inputs select which one of the data inputs is transmitted to the output. The logic equation for the 4-to-1 MUX is **F = A′B′I0 + A′BI1 + AB′I2 + ABI3.** Use the VHDL statement to model the MUX. **(7marks)**

(c). State the VHDL code for the three gates that have the signal A as a common input as given below. Gate 1, 2 and 3 have different delay times of 2ns, 1ns and 3ns respectively. **(4marks)**


B
1
D
A
2
E
3
F
C