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(University of Choice)

MASINDE MULIRO UNIVERSITY OF SCIENCE AND TECHNOLOGY (MMUST)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS 2021/2022 ACADEMIC YEAR

SECOND YEAR SECOND SEMESTER EXAMINATIONS

FOR THE AWARD OF DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING

COURSE CODE: DEE 077

COURSE TITLE: DIGITAL ELECTRONICS

DATE: Tuesday 26th April, 2022 **TIME:** 12 .00 pm – 2.00 pm

INSTRUCTIONS TO CANDIDATES

Question ONE (1) is compulsory
Answer Any Other TWO (2) questions
TIME: 2 Hours

QUESTION ONE (COMPULSORY)
(30MARKS)

a) Define the following terms in relation to Digital Electronics
   i. Logic gate
   ii. Combinational logic circuit
   iii. Sequential logic circuit

(3 marks)

b) Convert the following to binary numbers
   i. $(256.6875)_{10}$
   ii. $(AB)_{16}$

(4 marks)

c) Perform the following operations
   i. 3250-7230 using 10's complement
   ii. 1010101-1001111 using 2's complement

(4 marks)

d) Using relevant diagrams, ***explain*** three types of ***basic*** logic gates.

(6 marks)

e) Simplify the expression $(X\overline{Y} + Z)(X + \overline{Y})Z$ and give your answer as sum of products.

(4 marks)

f) With an aid of a well labelled diagram, **explain** the working of a binary adder.

(5 marks)

g) State the difference between the following logic circuits
   i. Decoder and Demultiplexer
   ii. Encoder and Multiplexer

(2 marks)

h) State any ***two*** uses of pulse of pulse generator.

(2 marks)

QUESTION TWO

a) Find the decimal equivalence of the following binary numbers.
   i. 01101110
   ii. 11101110
   (2 marks)

b) Define an Excess-3 BCD code. State the shortcoming of the 8421 code which is overcome in the Excess-3 code. Illustrate with the help of an example
   (3 marks)

c) Using a well labeled diagram, explain the operation of encoders. State any ***two*** major limitations of encoders
   (5 marks)

d) Construct a **5:32** line decoder with four **3:8** decoders with Enables and a **2:4** line decoder. Use block diagrams for components. *(10 marks)*

QUESTION THREE

a) Given the truth table below, by use of a K-map, derive the minimized SOP equation of the function F. Draw the circuit representation of the equation. *(7 marks)*

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

b) Define a Flip Flop in relation to digital electronics. State any two differences between a Latch and a Flip Flop.
   (4 marks)

e) State any ***three*** differences between synchronous and asynchronous counters.
   (6marks)

QUESTION FOUR

a) Differentiate between a register and a counter

(2 marks)

b) With the help clocked JK flip flops and waveform, explain the working of a three-bit binary ripple counter. Write truth table for clock transitions.

(12 *marks)*

i) With an aid of a well labelled diagram, **discuss** the ***two*** types of SR Latch.

(6 marks)

QUESTION FIVE

a) With the aid of a **1:4** as an example, explain the working of a demultiplexer.

(6 *marks)*

b) Discus how error is detected in communication systems.

(6 *marks)*

c) Register A and B contain four D-type flip flops each triggered at the positive edge of the clock pulse. Design a digital circuit that will transfer the data from Register A to Register B with a transfer command.

(8 *marks)*