(University of Choice)

MASINDE MULIRO UNIVERSITY OF SCIENCE AND TECHNOLOGY (MMUST)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS
2021/2022 ACADEMIC YEAR

FOURTH YEAR SECOND SEMESTER SPECIAL/SUPPLEMENTARY EXAMINATIONS

FOR THE DEGREE
OF
BACHELOR OF SCIENCE IN ELECTRICAL AND COMMUNICATION ENGINEERING

COURSE CODE: ECE 423

COURSE TITLE: MICROPROCESSOR SYSTEMS DESIGN

DATE: Friday, 07th October, 2022 **TIME: 12.00 - 02.00 p.m**

INSTRUCTIONS TO CANDIDATES

Answer Question ONE and any other TWO (2) questions

Marks will be awarded for correct working even if the answer is wrong

MMUST observes ZERO tolerance to examination cheating

This Paper Consists of 2 Printed Pages. Please Turn Over.

Question 1

a) State two advantage and two disadvantage of dynamic RAM over the static RAM. [4marks]

b) Using a block diagram explain 3 functions of the Keyboard/Display Controller 8279 interface chip. [6 marks]

c) If the mode register of 8251 contains 7FH, determine the format of transmitted characters. If the baud rate for transmitter and receiver are required to be 1200 and 300 respectively, then determine the frequencies to be applied to TXC and RXC to get the desired baud rate. [4marks]

d) An 8251A is interfaced to an 8086 microprocessor system in memory mapped I/O. Draw the logic diagram of the set up. [4marks]

e) Explain briefly the following communication techniques
   i. Simplex transmission [2 marks]
   ii. Duplex transmission [2 marks]
   iii. Half-duplex transmission [2 marks]

f) Compare I/O mapped and memory mapped I/O [6 marks]

Question 2

(a) Differentiate between hardware and software key debouncing for keyboard interface with the microprocessor. [3marks]

(b) Explain briefly the transparent or hidden transfer direct memory access method [4marks]

(c) Explain the following modes of the Programmable Peripheral Interface chip, 8255

(i) Bit set reset (BSR) [4marks]

(ii) I/O mode [3marks]

(d) Describe the numeric displays used in microprocessor systems [6marks]

Question 3

(a) Differentiate between static and dynamic random access memory [4marks]

(b)With the aid of a well labelled diagram, explain how an EPROM can be interfaced with an 8086 microprocessor. [4marks]

(c) Using well labelled diagrams, explain how the following memory capacities can be obtained by proper interconnection of decoder and memory ICs.

(i) 2K X 8 bits memory using two 1K X 8 bits memory [4marks]

(ii) 1K X 4 bits RAM for 1K byte RAM [4marks]

(d) Explain how address decoding is done using a 3 to 8 line decoder for an EPROM memory interface to the 8086 microprocessor. [4marks]

Question 4

(a) Write programs to perform the following operations of the Programmable Peripheral Interface chip, 8255.

(i) Reset bit 7 of port C [2marks]

(ii) Set bit 5 of port C [2marks]

Assume address of Port A=80H, Port B=82H, Port C=84H and CWR=86H.

(b) Explain briefly the input modes of the programmable display and keyboard controller, 8279.
[7marks]

(c) Determine the keyboard/display command word for the following specifications; 3 X 8 matrix keyboard- 2 key lock out and 6 digit display – left entry.
[4marks]

(d) When an interrupt is acknowledged, the processor goes through a sequence of events before executing the interrupt service. Give that sequence of operations in a microprocessor. [5marks]

Question 5

(a) Briefly explain the serial data transmission. [4marks]

(b) Using a schematic diagram explain

i. Asynchronous data transmission. [4marks]

ii. Synchronous data transmission. [4marks]

(c) Explain the data transfer modes of the Programmable Peripheral Interface chip, 8255.

(i) Interrupt driven input [4marks]

(ii) Status driven [4marks]