300

(University of Choice)

MASINDE MULIRO UNIVERSITY OF

SCIENCE AND TECHNOLOGY

(MMUST)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS

MAIN EXAM

2022/2023 ACADEMIC YEAR

SECOND YEAR FIRST SEMESTER EXAMINATION

FOR THE DEGREE OF BACHELOR OF SCIENCE IN INFORMATION TECHNOLOGY AND SONAS

COURSE CODE: BIT 212

COURSE TITLE: PLATFORM TECHNOLOGIES II

DATE: 07/12/2022 TIME: 2HRS 8:00 – 10:00 AM

INSTRUCTIONS TO CANDIDATES:

SECTION A IS COMPULSORY. ANSWER ANY OTHER TWO QUESTIONS IN SECTION B

TIME: 2 Hours

MMUST observes ZERO tolerance to examination cheating

SECTION A [COMPULSORY]: 30 MARKS

QUESTION 1

a) What do you understand by this assembly language instruction: ADD 5? [2 Marks]

b) Describe with the aid of a diagram the register indirect addressing [2 Marks]

c) Interrupt handling offers better efficiency, however there is some overhead experienced. Describe the overhead. [4 Marks]

d) On the IAS, describe in English the process that the CPU must undertake to read a value from memory and to write a value to memory in terms of what is put into the MAR, MBR, address bus, data bus, and control bus. [4 Marks]

e) What are the differences between DRAM and SRAM with regard to characteristics such as speed, size, and cost? [3 Marks]

f) Given the following code segment, provide the Assembly language equivalent: English: W divide by Y times D plus 10 and assign the results to X. [4 Marks]

g) Computer systems must have ways in which it can detect and correct errors. Describe either ODD or EVEN Parity and show how it is used to detect and correct errors in a computer system. [3 Marks]

h) Convert the following numbers in both Sign Magnitude and Two's Complement. Leave your answers in 8bit notation, 18, -18, -32658. [3 Marks]

i) Assume that you were running a number of applications on your mobile phone then all of a sudden, the phone becomes considerably slow. It then sends an error message that "the phone is running out of space" yet when you check the storage, you find that there is some space remaining though not a lot. Why is your mobile phone giving this kind of error? What is the short term and long term solution to this problem? [5 Marks]

QUESTION 2

a. What are the differences among sequential access, direct access, and random access? [6 Marks]

b. Mathematically, it is known that -7x3=-21. The computer's ALU uses many models to effect such arithmetic functions. Using the Booth algorithm, clearly show how the above mentioned calculation is conducted to realize the answer. [12 Marks]

c. What are the four essential elements of a number in floating-point notation? [2 Marks]

QUESTION THREE [20 MARKS]

a. State any five functions of the I/O module [8 Marks]
b. List and briefly define the various techniques implemented by computer designers for performing peripheral functions. [6 Marks]
c. There are four design issues defined that the processor uses in determining which I/O device sent an interrupt? Briefly explain a notable disadvantage in each of the designs.

d. Divide - 145 by 13 in binary twos complement notation, using 12-bit words. [4 Marks]

e. How is RAID important in storage systems. [2 Marks]

QUESTION FOUR [20 MARKS]

a. Describe the following bus arbitration addressing modes: [9 Marks]
   - Memory mapped I/O
   - Isolated I/O

b. With the aid of a diagram, describe the instruction cycle that implements interrupts. [6 Marks]
c. What are the differences among sequential access, direct access, and random access? [3 Marks]
d. Why is cache memory important? [2 Marks]

QUESTION FIVE [20 MARKS]

A processor accesses main memory with an average access time of T_2. A smaller cache memory is interposed between the processor and main memory. The cache has a significantly faster access time of $T_1 < T_2$. The cache holds, at any time, copies of some main memory words and is designed so that the words more likely to be accessed in the near future are in the cache. Assume that the probability that the next word accessed by the processor is in the cache is H, known as the hit ratio.

a. For any single memory access, what is the theoretical speedup of accessing the word in the cache rather than in main memory? [4 Marks]
b. Let T be the average access time. Express T as a function of T_1, T_2, and H. What is the overall speedup as a function of H? [4 Marks]
c. In practice, a system may be designed so that the processor must first access the cache to determine if the word is in the cache and, if it is not, then access main memory, so that on a miss (opposite of a hit), memory access time is $T_1 + T_2$. Express T as a function of T_1, T_2, and H. Now calculate the speedup and compare to the result produced in part (b). [6 Marks]
d. Define the terms *seek time, rotational delay, access time,* and *transfer time.* [6 Marks]