



MASINDE MULIRO UNIVERSITY OF SCIENCE AND TECHNOLOGY (MMUST)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS 2023/2024 ACADEMIC YEAR

THIRD YEAR FIRST SEMESTER EXAMINATIONS

FOR THE DEGREE OF BACHELOR OF SCIENCE IN ELECTRICAL AND COMMUNICATION ENGINEERING

COURSE CODE: ECE 316

COURSE TITLE: DIGITAL ELECTRONICS 1

DATE: MONDAY 11/12/2023 TIME: 3: 00 PM - 5:00 PM

INSTRUCTIONS TO CANDIDATES

Question ONE (1) is compulsory Answer Any Other TWO (2) questions

TIME: 2 Hours

MMUST observes ZERO tolerance to examination cheating

QUESTION ONE (COMPULSORY) (30MARKS)

- a) Distinguish between the following terms
 - i. Combinational logic circuit and Sequential logic circuit
 - ii. Minterms and Maxterms

(4 marks)

- b) Convert the following to binary numbers
 - i. (64.6875)₁₀
 - ii. (DF)₁₆

(4 marks)

c) Given two binary numbers X=1010100 and Y=1000011, perform the subtraction (a)
 X-Y and (b) Y-X using 2's complements

(4 marks)

d) Prove the Consensus law X.Y + X'.Z + Y.Z = X.Y + X'Z

(3 marks)

e) With an aid of a well labelled diagram, explain the working of a binary adder.

(4 marks)

f) State any three differences between synchronous and asynchronous counters.

(3 marks)

g) With an aid of a well labelled diagram, discuss the two types of SR Latch.

(4 marks)

h) Define a pulse generator and give its two areas of application.

(4 marks)

QUESTION TWO

a) Convert 101110112 to its equivalent Gray code.

(2 marks)

b) Define an Excess-3 BCD code. State the shortcoming of the 8421 code which is overcome in the Excess-3 code. Illustrate with the help of an example

(3 marks)

c) Using a well labeled diagram, explain the operation of multiplexers. State any *two* major limitations of Multiplexers.

(5 marks)

d) Construct a **5:32** line decoder with four **3:8** decoders with Enables and a **2:4** line decoder. Use block diagrams for components

(10 marks

QUESTION THREE

a) i) With the aid of a circuit diagram and a truth table, explain the working of a full subtractor. (5 marks)

ii) By use of a K-map, derive the minimized SOP equations for the functions D and Bo.

(5 marks)

b) Define a Flip Flop in relation to digital electronics. State any two differences between a Latch and a Flip Flop.

(4 marks)

c) With an aid of an appropriate diagram, briefly discuss any two types of Flip Flops

(6 marks)

QUESTION FOUR

a) Differentiate between a register and a counter

(2 marks)

- b) With an aid of a well labelled diagram, describe the working of a 4-bit SISO register (8 marks)
- c) With the help clocked JK flip flops and waveform, explain the working of a three-bit binary ripple counter. Write truth table for clock transitions.

(10 marks)

QUESTION FIVE

a) i) State the difference between a demultiplexer and a decoder. (2 marks)

ii) Implement a 1:16 Demultiplexers using lower order Demultiplexers.

(8 marks)

b) Register A and B contain four D-type flip flops each triggered at the positive edge of the clock pulse. Design a digital circuit that will transfer the data from Register A to Register B with a transfer command. (10 marks)