(*University of Choice*)

MASINDE MULIRO UNIVERSITY OF SCIENCE AND TECHNOLOGY (MMUST)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS 2023/2024 ACADEMIC YEAR

THIRD YEAR FIRST SEMESTER MAIN EXAMINATIONS

FOR THE DEGREE OF BACHELOR OF SCIENCE IN ELECTRICAL AND COMMUNICATIONS ENGINEERING

COURSE CODE: ECE 314

COURSE TITLE: ANALOGUE ELECTRONICS I

DATE: TUESDAY 05/12/2023 **TIME: 3.00 PM - 5.00 PM**

INSTRUCTIONS TO CANDIDATES

Question ONE (1) is compulsory
Answer Any Other TWO (2) questions

TIME: 2 Hours

MMUST observes ZERO tolerance to examination cheating

This Paper Consists of 4 Printed Pages. Please Turn Over.

QN 1 [30mks]

(a) With regards to amplifiers, distinguish between each of the following circuits; **[2mks]**

i) Direct Coupled and RC coupled amplifiers

ii) Class A and class B amplifiers

(b) Consider the amplifier circuit of **Fig.1**

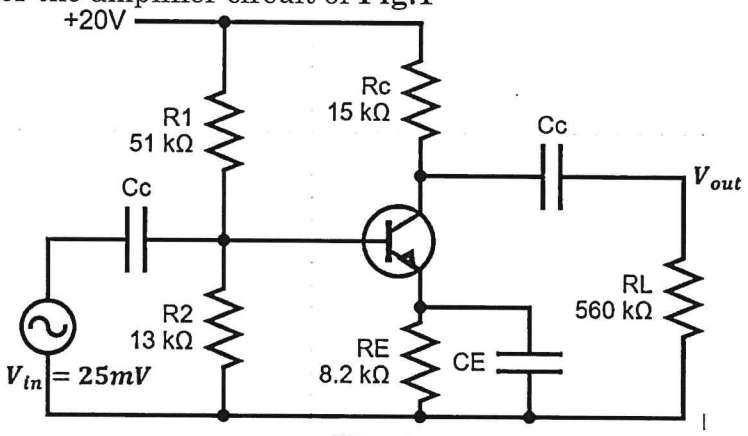

Fig. 1

i) Draw the small signal Hybrid equivalent circuit for **Fig.1** **[2mks]**

ii) Given that: $h_{re} \approx 2.5 \times 10^{-4}, h_{oe} \approx 25\mu S, h_{fe} = 50, h_{ie} = 1000\Omega$.
Calculate:

i) Input impedance of the amplifier stage **[3mks]**

ii) Output impedance of the amplifier stage **[3mks]**

iii) Voltage gain (A_v) **[2mks]**

iv) Current gain (A_i) **[2mks]**

(c) For the circuit of **Fig. 1**, $V_{BE} = 0.7V, V_{CC} = +20V$, determine:

i) the d.c. loadline **[1mk]**

ii) The operating point **[2mks]**

iii) The a.c. loadline **[2mks]**

iv) Sketch the DC and ac loadlines on the same graph **[1mk]**

(d) Considering **Fig. 1** as class A, large-signal amplifier circuit.
Calculate the:

i) Input power **[1mk]**

ii) Output power **[1mk]**

iii) Efficiency of the amplifier **[1mk]**

(e) For **Fig. 1**, given that $\beta_{ac} = 200, V_{BE} = 0.7V, V_{in\,(ac)} = 25mV, V_{CC} = +20V$; determine the following:

i) Voltage gain **[2mks]**

ii) Current gain **[4mks]**

iii) Power gain **[1mk]**

QN 2 [20mks]

(a) Using a well labeled output characteristic curve, explain how a JFET operates as a **constant resistor** and a **constant current** source. **[10mks]**

(b) The N-channel JFET of **Fig. 2** has the following parameters on the data sheet: $V_{DD} = 20V$; $V_{GSQ} = -2.6V$; $I_{DQ} = 2.6mA$; $I_{DSS} = 8mA$; $V_P = -6V$; $g_{os} = 20\mu S$; $V_{GS} = -4.5V$; $V_D = 12V$

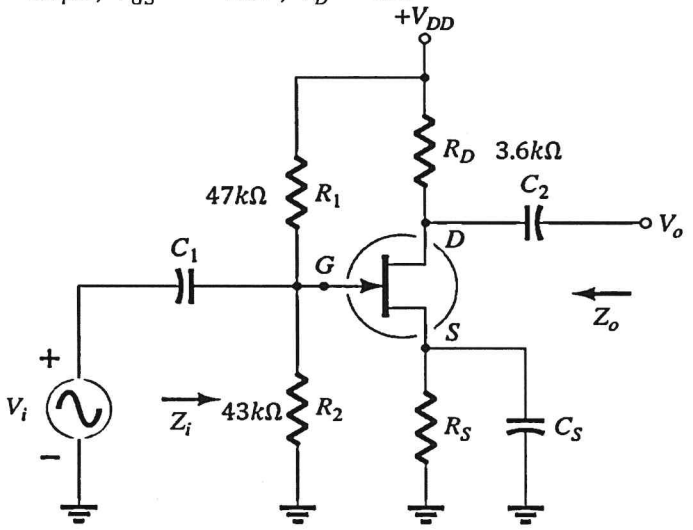

Fig. 2

(c) Determine the following:

i) The source resistance R_S **[4mks]**

ii) Transconductance (gm). **[2mks]**

iii) Drain-source resistance (r_d) **[1mk]**

iv) Input impedance (Zi) **[1mk]**

v) Output impedance (Z_o) with the effects of r_d **[1mk]**

vi) Voltage gain (A_V) **[1mk]**

QN 3 [20mks]

(a) *i)* State TWO salient features of class B amplifiers. **[2mks]**

ii) Draw the circuit diagram of a typical class B push -pull amplifier and explain how it works. **[3mks]**

iii) Describe cross-over distortion in class B amplifiers using well labelled output waveforms. **[3mks]**

iv) Using a circuit diagram, describe how cross-over distortion is eliminated in class B amplifiers. **[3mks]**

(b) A class B amplifier delivers a $20V$ peak signal to a 16Ω speaker and a power supply of $V_{CC} = 30V$, determine:

i) The input power. **[1mk]**

ii) **Maximum** input power. **[1mk]**

iii) Output power delivered to the load. **[1mk]**

iv) **Maximum** output power delivered to the load. **[1mk]**

v) Amplifier circuit efficiency. **[1mk]**

vi) **Maximum** amplifier efficiency. **[1mk]**

vii) Power dissipated by both transistors at maximum power input and output conditions. **[1mk]**

viii) **Maximum** power dissipated by both transistors **[1mk]**

ix) The corresponding input voltage for maximum power dissipation by both transistors. **[1mk]**

QN 4 [20mks]

(a) A class C tuned amplifier circuit diagram in **Fig. 3** has the following components: $C = 0.125\mu F, L = 25mH, R = 30k\Omega$.

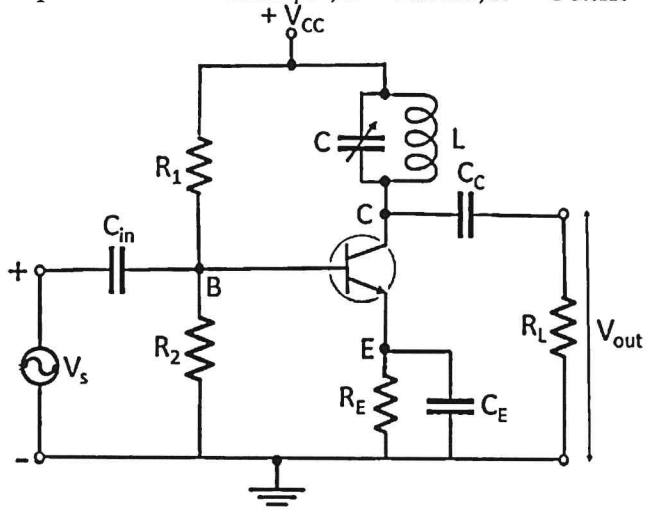

Fig. 3

Determine:

i) The resonant frequency. **[2mks]**

ii) Quality factor Q of the tank circuit. **[3mks]**

iii) Bandwidth of the amplifier. **[1mk]**

(b) Consider a two-stage RC-coupled amplifier network in **Fig. 4**

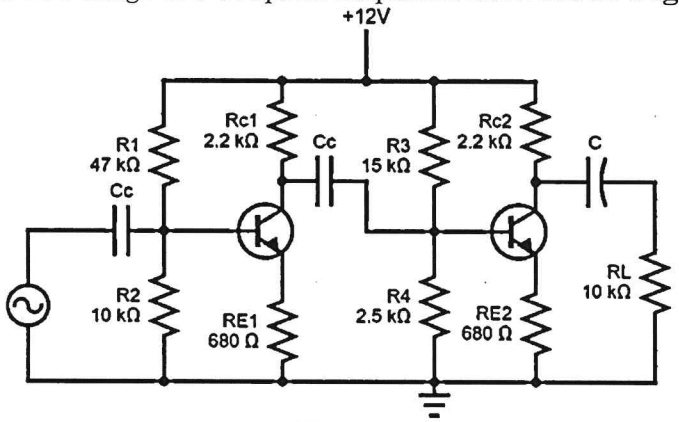

Fig. 4

Determine the following:

i) Dynamic emitter resistances for the 1st and 2nd stages **[8mks]**

ii) Voltage gain for the first stage of the network. **[4mks]**
[Take $\beta_{ac2} = 160$]

iii) Overall gain **[3mks]**

QN 5 [20mks]

(a) By using circuit diagrams, describe the basic difference between the Colpitts and Hartley oscillators. **[4mks]**

(b) With aid of circuit diagram, describe the operation of the RC Phase-Shift Oscillator. **[5mks]**

(c) A phase shift oscillator with three RC stages uses 5 pF capacitors. Find the resistance values that produce a frequency of 800 kHz. **[3mks]**

(d) Design a Hartley oscillator with appropriate inductor values such that the operating frequency, $f = 1.5MHz$, the feedback fraction $\beta = 0.2$, and a 1pF capacitor on the feedback circuit. **[8mks]**