(University of Choice)

MASINDE MULIRO UNIVERSITY OF SCIENCE AND TECHNOLOGY (MMUST)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS 2023/2024 ACADEMIC YEAR

FOURTH YEAR SECOND SEMESTER EXAMINATIONS

FOR THE DEGREE

OF

BACHELOR OF TECHNOLOGY EDUCATION IN ELECTRICAL AND ELECTRONIC ENGINEERING

COURSE CODE: TEE 322

COURSE TITLE: ANALOGUE ELECTRONICS II

DATE: FRIDAY, APRIL 12TH 2024 **TIME:** 15:00 PM - 17:00 PM

INSTRUCTIONS TO CANDIDATES

i) Question **ONE (1)** is compulsory
ii) Answer Any Other **TWO (2)** questions

TIME: 2 Hours

MMUST observes ZERO tolerance to examination cheating

QN 1 [30mks]

(a) **i)** State the reason why voltage divider bias is preferred over other biasing techniques. [1mk]

ii) Explain the importance of each of the following components in multistage amplifiers;

i) Emitter resistor [1mk]

ii) Bypass capacitor [1mk]

iii) Coupling capacitors [2mks]

iv) Biasing voltage (Vcc) [2mks]

(b) State TWO differences between each of the following:

i) FETs and BJTs [2mks]

ii) BJT based phase shift and Wein bridge oscillators [2mks]

iii) Inverting and non-inverting Op-amps [2mks]

(c) For the circuit in **Fig. 1**, derive the equation for the closed loop gain. [3mks]

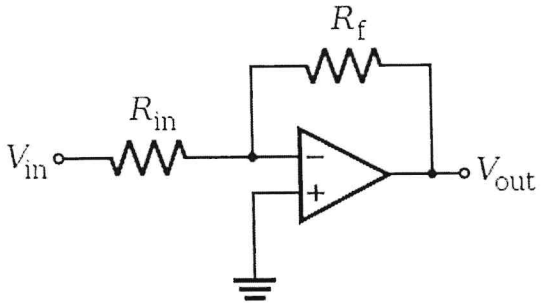


Fig. 1

(d) The BJT in the circuit of **Fig. 2** has the following values $V_{BE} = 0.7V, \beta_{ac} = 200$.

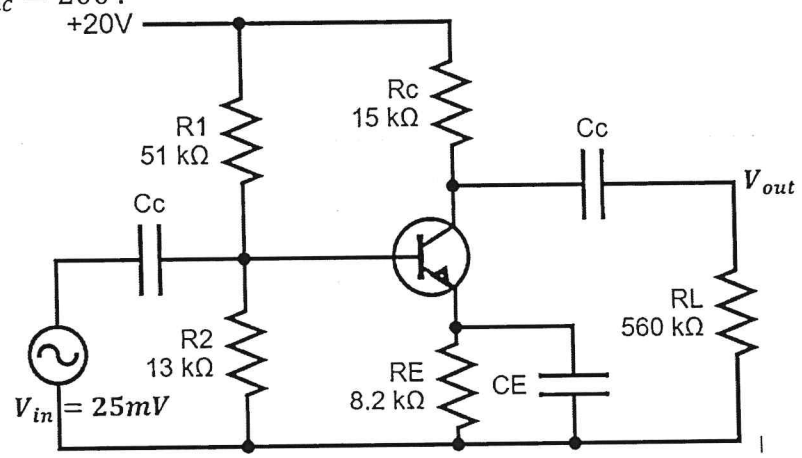


Fig. 2

Determine:

i) the d.c. loadline [1mk]

ii) The operating point [3mks]

iii) The a.c. loadline [2mks]

iv) Sketch the DC and ac loadlines on the same graph [1mk]

v) Voltage gain [2mks]

vi) Current gain [4mks]

vii) Power gain [1mk]

QN 2 [20mks]

(a) Using a well labeled output characteristic curve, explain how a JFET operates as a **constant resistor** and a **constant current** source. [8mks]

(b) The N-channel JFET of **Fig. 3** has the following parameters on the data sheet:$V_{DD} = 20V; I_{DSS} = 8mA; V_P = -6V;\ g_{os} = 20\mu S;\ V_{GS} = -4.5V;\ R_s = 12.6k\Omega$

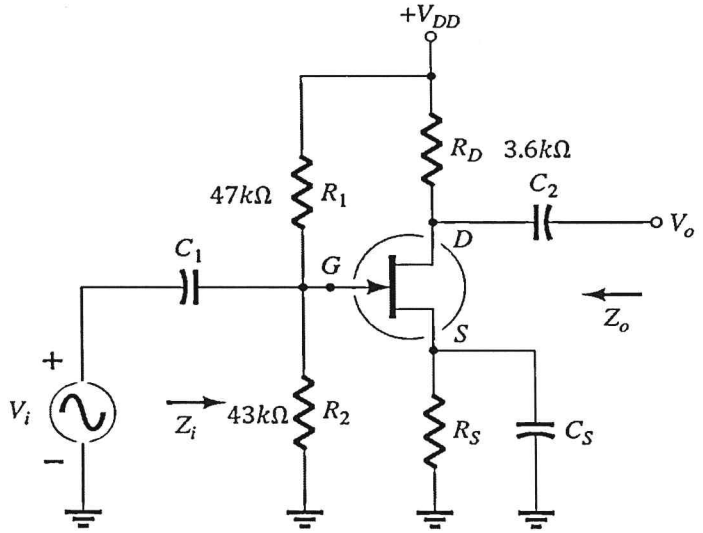


Fig. 3

(c) Determine the following:

i) the d.c. loadline [1mk]

ii) The operating point [3mks]

iii) The a.c. loadline [2mks]

iv) Sketch the DC and ac loadlines on the same graph [2mks]

v) Transconductance (gm) [2mks]

vi) Input impedance (Zi) [1mk]

vii) Voltage gain (A_V) [1mk]

QN 3 [20mks]

(a) By using circuit diagrams, describe the basic difference between the Colpitts and Hartley oscillators. [4mks]

(b) With aid of circuit diagram, describe the operation of the RC Phase-Shift Oscillator. [5mks]

(c) A phase shift oscillator with three RC stages uses 5 pF capacitors. Find the resistance values that produce a frequency of 800 kHz. [3mks]

(d) Design a Hartley oscillator with appropriate inductor values such that the operating frequency, $f = 1.5MHz$, the feedback fraction $\beta = 0.2$, and a 1pF capacitor on the feedback circuit. [8mks]

QN 4 [20mks]

(a) *i)* State THREE reasons why series voltage regulators are preferred over shunt regulators. [3mks]

ii) With aid of circuit diagram, explain how a transistor series voltage regulator maintains the output voltage regardless of variations. [3mks]

iii) A series voltage regulator is required to supply a current of 1A at a constant voltage of 6V. If the supply voltage is 10V,$\beta = 50, V_{BE} = 0.5V, I_{Z(min)=}\ 10mA$ and the zener operates in the breakdown region, design the circuit. [4mks]

(b) Consider a two-stage RC-coupled amplifier network in **Fig. 4**

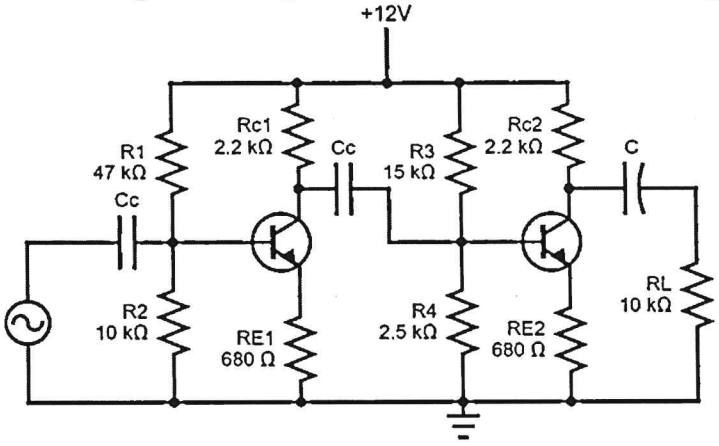


Fig. 4

Determine Dynamic emitter resistances for the 1st and 2nd stages [10mks]

QN 5 [20mks]

(a) **i)** Define the following terms: [4mks]

i) Virtual ground

ii) Input offset current

iii) Common-Mode Rejection Ratio

iv) Slew rate

ii) State FOUR practical Op-Amp characteristics [4mks]

(b) The circuit in **Fig. 5** shows a non-inverting amplifier with a supply voltage of $5V$ at the non-inverting input terminal.

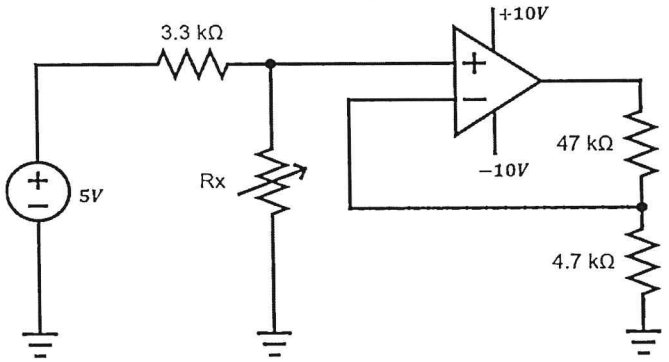


Fig. 5

i) Find the output voltage if the variable resistor $R_x = 8\text{k}\Omega$ [3mks]

ii) Determine the maximum value of R_x for the Op-Amp to avoid saturation. [4mks]

Consider the circuit in **Fig. 6**, where $C = 6\mu F, R = 3.3k\Omega$.

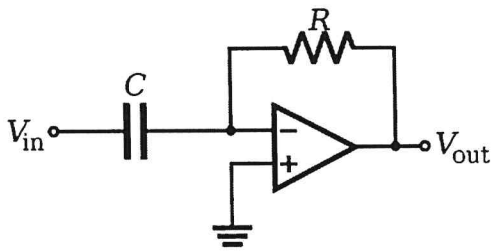


Fig. 6

(c) Determine the output voltage, if the input voltage is $V_{in} = 5\cos(100t)$ [4mks]

(d) Sketch the output waveform [1mk]